CLAIMS

What is claimed is:

1. A data processing system, comprising:

one or more processing cores; and

a memory controller, coupled to said one or more processing cores, that controls access to a system memory containing a plurality of rows, said memory controller having a memory speculation table that stores historical information regarding prior memory accesses, wherein said memory controller includes:

means, responsive to a memory access request, for directing an access to a selected row among the plurality of rows in the system memory to service the memory access request; and

means for speculatively causing the system memory to continue to energize said selected row following said access based upon said historical information in said memory speculation table.

2. The data processing system of Claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.

3. The data processing system of Claim 1, wherein said memory speculation table stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

4. The data processing system of Claim 1, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said memory speculation table stores

said historical information on a per-bank basis.

5. The data processing system of Claim 1, wherein said plurality of rows are organized in one or more banks, and wherein said means for speculatively continuing to energize said selected row comprises means for speculatively continuing to energize said selected row until a next access to another row within a same bank as said selected row.

6. The data processing system of Claim 1, wherein:

said system memory comprises a first system memory;

said memory controller comprises a first memory controller;

said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory; and

said means for speculatively continuing to energize said selected row comprises means for speculatively continuing to energize said selected row based upon historical information recorded by said second memory controller.

7. The data processing system of Claim 1, and further comprising:

a system interconnect coupling said plurality of processing cores; and

one or more cache hierarchies coupled to said plurality of processing cores that cache data from said system memory.

8. A memory controller for controlling a system memory of a data processing system, wherein the system memory includes a plurality of rows, said memory controller comprising:

a memory speculation table that stores historical information regarding prior memory accesses;

means, responsive to a memory access request, for directing an access to a selected row among the plurality of rows in the system memory to service the memory access request; and

means for speculatively causing the system memory to continue to energize said selected row following said access based upon said historical information in said memory speculation table.

9. The memory controller of Claim 8, wherein said memory speculation table stores a respective memory access history for each of a plurality of threads executing within said data processing system.

10. The memory controller of Claim 8, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said memory speculation table stores said historical information on a per-bank basis.

11. The memory controller of Claim 8, wherein said plurality of rows are organized in one or more banks, and wherein said means for speculatively continuing to energize said selected row comprises means for speculatively continuing to energize said selected row until a next access to another row within a same bank as said selected row.

12. The memory controller of Claim 8, wherein:

said means for speculatively continuing to energize said selected row comprises means for speculatively continuing to energize said selected row based upon historical information recorded by another memory controller.

13. A method of operating a memory controller of a system memory of a data processing system, wherein the system memory contains a plurality of rows, said method comprising:

said memory controller storing historical information regarding prior memory accesses in a memory speculation table;

in response to receipt of a memory access request, directing an access to a selected row among the plurality of rows in the system memory to service the memory access request; and

speculatively directing the system memory to continue to energize said selected row following said access based upon said historical information in said memory speculation table.

14. The method of Claim 13, wherein said storing comprises storing a respective memory access history for each of a plurality of threads executing within said data processing system.

15. The method of Claim 13, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said storing comprises storing said historical information in said memory speculation table on a per-bank basis.

16. The method of Claim 13, wherein said plurality of rows are organized in one or more banks, and wherein said step of speculatively continuing to energize said selected row comprises speculatively continuing to energize said selected row until a next access to another row within a same bank as said selected row.

17. The method of Claim 13, wherein said step of speculatively continuing to energize said selected row comprises speculatively continuing to energize said selected row based upon historical information recorded by another memory controller.